REPORT NO. P72-308R

CONTRACT NO. NAS8-28937

ELECTROMAGNETIC RADIATION SCREENING OF SEMICONDUCTOR DEVICES FOR LONG LIFE APPLICATIONS

Prepared for:
NASA/George C. Marshall
Space Flight Center
Huntsville, Alabama

DECEMBER 1972

AEROSPACE GROUP

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

Contract NAS8-28937

ELECTROMAGNETIC RADIATION SCREENING OF SEMICONDUCTOR DEVICES FOR LONG LIFE APPLICATIONS

December 1972

Thomas C. Hall
William G. Brammer

Equipment Engineering Divisions
AEROSPACE GROUP
Hughes Aircraft Company • Culver City, California

CONTENTS

CONTENTS (Continued)

LIST OF ILLUSTRATIONS

1.0 SUMMARY

Semiconductor devices for high reliability applications are subjected to 100 percent precap visual examination to screen out manufacturing defects. This is an effective screen, but is subject to human error. In addition with respect to chip flaws, only surface defects and gross bulk defects (cracks) are detected. This study determines the feasibility of using electromagnetic radiation as an effective comparison screen. Electromagnetic radiation creates photogenerated electrical carriers (i.e., holes and electrons) which produce electrical signals at the device terminals. These signals will vary, depending upon the presence of various defects in the finished semiconductor device. Such signals, sensed while the device is undergoing electrical tests, could be analyzed to produce a set of characteristic identifying fingerprints associated with the various defects that might occur in the device.

The first part of this study constitutes a review, in some detail, of the mechanism of interaction of electromagnetic radiation in various spectral ranges, with various semiconductor device defects. Previous work conducted in this area has been analyzed as to its pertinence to the current problem.

The second part of the study encompasses a review of the task of implementing electromagnetic screening methods in the wavelength region determined to be most effective in the first part. Both scanning and flooding type stimulation techniques are discussed. While the scanning technique offers a considerably higher yield of useful information, a preliminary investigation utilizing the flooding approach is first recommended because of the ease of implementation, lower cost and ability to provide go-no-go information in semiconductor screening.

Through the methods investigated here, it appears possible to stimulate a semiconductor device with electromagnetic radiation while observing the electrical performance and thereby obtain quality information that is unavailable through other non-destructive techniques. Such an inspection technique would augment rather than supplant present electrical and visual inspection procedures.

2.0 INTRODUCTION

The continuously increasing circuit complexity of electronic systems in general, coupled with the existence of a minimal or no-maintenance requirement for many such systems, particularly in long-life space applications, generates an ever increasing need for ultimate reliability of electronic components. This study deals with semiconductor components. In the semiconductor device fabrication process, some of the most important steps in the fabrication sequence are those which deal with inspection. It is during these critical operations that the inevitable errors in materials processing are detected and eliminated. Unfortunately, it is precisely these inspection steps which are most subjective and vulnerable to error since they are now performed principally by human operators. Visual inspection is never executed in exactly the same manner even when performed by the same operator. Further, many significant defects are not visible under practical production conditions.

Electrical tests are limited to those parameters that are detectable at the device terminals and can be stimulated through a reasonable combination of input signals. Electrical results usually relate to current device performance rather than dormant defects that may be stimulated through environment or operation in service.

A technique that offers the possibility of partially overcoming these inspection limitations has been recommended. The technique utilizes electromagnetic radiation to excite a semiconductor while monitoring the electrical performance at the device terminals. Through this technique, portions of a device that are otherwise accessible only with probes can be activated and exercised. The technique has the potential of sensing visually undetectable

subsurface flaws thus aiding in providing go-no-go information in semiconductor device screening.

The purposes of this study are:

1. Study the interactions of electromagnetic radiation with semiconductor devices and investigate the applicability of these interactions and their secondary effects to the detection of selected semiconductor anomalies.
2. Investigate the methods and equipment needed to implement an electromagnetic radiation screening system.
3. Recommend possible further work as warranted by the results of this study.

3.0 MATERIAL AND PROCESS RELATED FLAWS IN SEMICONDUCTOR DEVICES

In view of the basic objective of this study, namely to suggest means for detecting process and material related flaws in semiconductor devices by employing electromagnetic radiation, some discussion of the nature of such flaws is important. In this section such flaws are related to modification of material properties and subsequent degradation in device electrical characteristics. (Ref. 1)

During the intricate series of processes employed in generating a semiconductor device, the risk of introducing structural and/or impurity defects is high even under the best possible conditions of production process control. Such defects are introduced in addition to that irreducible minimum already existing in the best starting semiconductor wafer material. The production of high quality devices for applications demanding ultimate reliability necessitates the maximum possible understanding of the physical and chemical basis for the generation of such material and process related defects as well as their effects upon device performance and reliability.

3.1 Starting Material Errors

The input silicon starting material in a typical semiconductor process is subject to a number of types of structural and impurity errors. These may be classified into the following categories:

1. Crystal Structural Errors
   - a. Lattice vacancies
   - b. Dislocations
     - i. Edge
     - ii. Screw
   - c. Grain boundaries

2. Chemical Impurities
   a. N type (near conduction band)
   b. P type (near valence band)
   c. Neutral (midgap)
3. "Decoration" Effects (Interaction of No. 1 and No. 2)

There is a considerable overlap in the effect of the various above listed structural errors on bulk semiconductor electrical properties, including electrical resistivity value, conductivity type (N and P), and hole/electron lifetime. Ultimately, of course, these effects will modify device electrical performance and reliability. In order to understand the effects of crystal structure errors and impurities, an understanding of energy band structure of semiconductors is essential.

In Figure 1 is presented an energy band diagram for a typical semiconductor (e. g., silicon), showing the case of an "intrinsic" semiconductor. The valence band, the conduction band and the forbidden gap with the Fermi level at midgap position terminate at the crystal surface in a perpendicular fashion, indicating no difference in electrical properties between the bulk material and the surface material.

In Figure 2 (A-F) are shown the six possible cases of surface enhancement, depletion and inversion layers on both N and P type bulk material. In the case of the depletion layer (Figure 2, C and D), the surface resistivity is effectively decreased. In the case of the enhancement layer (Figure 2, A and B), the surface resistivity is increased. In the case of the inversion layer (Figure 2, E and F), the surface resistivity has been increased through the intrinsic condition and inverted in conductivity type at the surface from N or P or P to N, respectively. Such shifts in Fermi level energy are a measure of changes in electronic state density within the crystal at or near the surface. Such states may be produced by either specific atomic impurities or by crystal structural errors (e. g., dislocations, lattice vacancies, etc.). A simple bell distribution curve shows the energy distribution of the surface states in each case. In actuality, such distribution curves are quite complex and variable in shape in relation to varying chemical ambient impurity and related surface condition. Changes in the surface Fermi level, therefore,

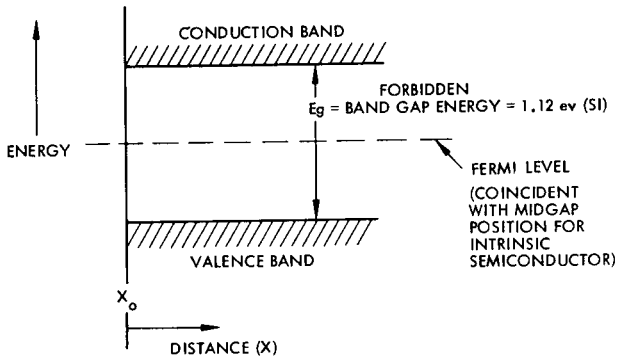

Figure 1. Energy band diagram for semiconductor at surface (intrinsic case)

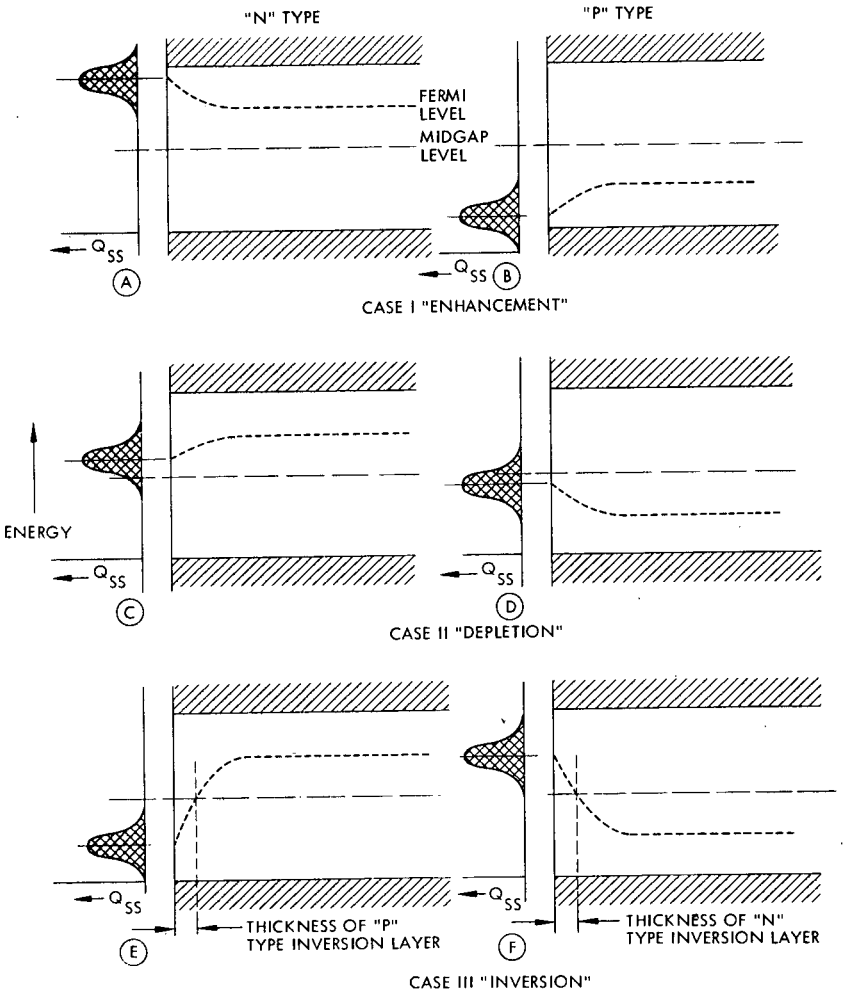

Figure 2. Semiconductor surface conductivity modifications due to flaws

do not always require the presence of N or P type or midgap impurities but may be produced by crystal structural faults.

In Figure 3 (A-F) is shown in a fashion analogous to the surface case discussed above the effects of a localized modification of bulk states due to a bulk flaw upon the Fermi level of the semiconductor in the immediate region of the flaw. As with Figure 2 above, six possible cases are included with enhancement, depletion and inversion for both N and P bulk material. In this diagram, it is evident that islands of enhanced or reduced sensitivity within the bulk as well as islands inverted conductivity type are possible due to inhomogeneities within the semiconductor crystal. Such inhomogeneities produce localized regions of modified conductivity magnitude and/or type.

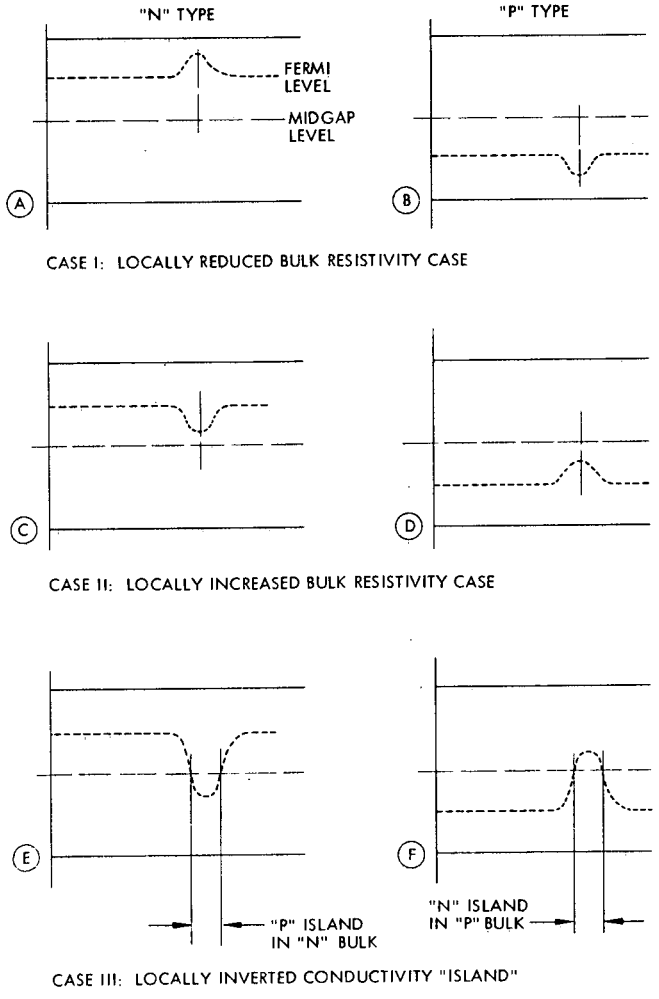

Figure 3. Semiconductor bulk conductivity modifications due to flaws

They can be produced by bulk structural or impurity errors introduced at any one of the many steps in the intricate wafer processing sequence. These possibilities and their consequences are discussed briefly in each of the ensuing sections.

3.2 Oxidation and Diffusion Process Faults

Oxidation of and impurity diffusion into the silicon wafer are the two most basic operations in fabrication of semiconductor devices by the universally used "planar" process. Both operations may be implemented in a wide variety of ways and under many varied combinations of time, temperature, and wafer chemical impurity and mechanical stress conditions.

The process of oxidation generates a silicon dioxide film on the wafer surface by diffusion of oxygen into the silicon until stoichiometric ratios are reached employing temperatures ranging from 800 to 1300°C. The thermal expansion coefficient difference between SiO_2 (quartz) (negligible) and silicon (significant) is sufficiently great to cause structural changes in the semiconductor surface upon cooling to room temperature. The SiO_2 layer in finished devices at room temperature is in compression and the surface Si material is in tension producing a mechanical stress at the interface. This condition will be relieved by any available mechanism including the creation of lattice vacancies and dislocations within the silicon at or near the interface. Such modifications are accompanied by the formation of surface states as well as superficial bulk states, the precise energy distribution and density of which will vary depending upon the details of oxide thickness, cooling rate, annealing time, ambient and bulk impurity condition, etc. The generation of surface state distributions which peak in the midgap position will, for example, modify the average carrier lifetime at the silicon surface as shown in Figure 2-C and 2-D. Donor and acceptor type surface states may also be generated and will have the net effect of modifying surface conductivity magnitude and type.

The process of impurity diffusion introduces selected impurities into the silicon lattice by filling thermally generated lattice vacancies. Solid diffusion is a lattice defect dependent process and in addition leads to the

production of structural flaws. Diffusion at sufficiently high surface concentrations (C_o) can lead to new chemical compound formation, for example SiO_2 with oxygen and Si_3B_4 (silicon boride) with elemental boron. Such compounds due to thermomechanical and silicon lattice mismatch will lead to localized mechanical stress which may be relieved by screw and edge dislocation and lattice vacancy formation. Such surface and bulk changes will in general have very significant effects upon the electrical performance and reliability of any device which may be fabricated with such a crystal. All of this points up the need to understand and control the physics and chemistry of semiconductor surfaces not only in finished devices but also for wafers in process.

3.3 Epitaxial Material Faults

A technique widely employed in semiconductor device fabrication is the epitaxial deposition process by which the crystal structure of the substrate wafer is grown to a desired additional thickness. The added material may be prepared in either N or P type conductivity type and with a wide range of resistivity values with any desired dopant impurity. Since the epitaxial deposition is accomplished under conditions of a low time-temperature product, the impurity gradients which exist in the wafer substrate and in the epitaxial layer are not greatly modified. This important virtue of epitaxy allows greater flexibility in device geometry selection and control than is afforded by conventional solid diffusion techniques. For this reason, it is employed in fabrication of certain devices of specialized or critical geometry.

Epitaxially grown semiconductor material tends to be higher in structural defect or "stacking fault" density than the substrate material upon which it is grown. Furthermore, it tends to become more "defective" as it is grown to ever greater thickness. This "cumulative error" property of epitaxial growth is due to certain basic chemical thermodynamic considerations relating to "non-equilibrium" processes. Epitaxial growth is accomplished at temperatures considerably below the melting point for the crystal which might be designated as an "equilibrium" temperature for

crystal growth. This fundamental limitation of epitaxial growth processes imposes limits upon feasible levels of epitaxial crystal perfection and useful film thickness.

In addition, since epitaxy is accomplished employing chemical vapor deposition methods, the inclusion of certain chemical impurities incidental to the chemistry employed provide additional sources of "error" in crystal impurity content. Such errors in crystal structure as well as in impurity condition will have their effects upon electrical carrier lifetime and conductivity magnitude and type in resultant device structures. These errors will in general modify the electrical characteristics and the photo response of junctions fabricated with such crystals.

4.0 ELECTROMAGNETIC RADIATION EFFECTS ON SEMICONDUCTOR DEVICES

4.1 General Discussion

The most significant physical process involved in the interaction of electromagnetic radiation with semiconductors of interest in this study, is the generation of hole-electron pairs within the semiconductor solid. Other more classical optical processes including diffraction, scattering, refraction and reflection are of course important and are also treated appropriately.

The interaction of photo-generated electrical carriers in a semiconductor device with the various electrical junctions contained therein is of principal interest and can be employed to assess the state of "perfection" of the overall device. A detectable signal is produced by the collection of these carriers at a given p-n junction to produce a photo-voltage across that junction. This photo-voltage will produce photo-currents in associated closed circuits in the device. The magnitude and time decay characteristics of the observed photovoltaic response may be employed to assess the existence and nature of "defects" in the device structure.

The existence of a structurally damaged region in a semiconductor device crystal, due to residual work damage from processing or incidental scratches in handling, will act as a "sink" for photo-generated carriers and will reduce the population of those carriers which survive to be collected by a nearby p-n junction. The photo response of such a junction in the damage locale will thus be diminished.

The role of a device process flaw (e.g., a surface scratch, etc.) in reducing the photo-response of a nearby p-n junction is illustrated in Figure 4.

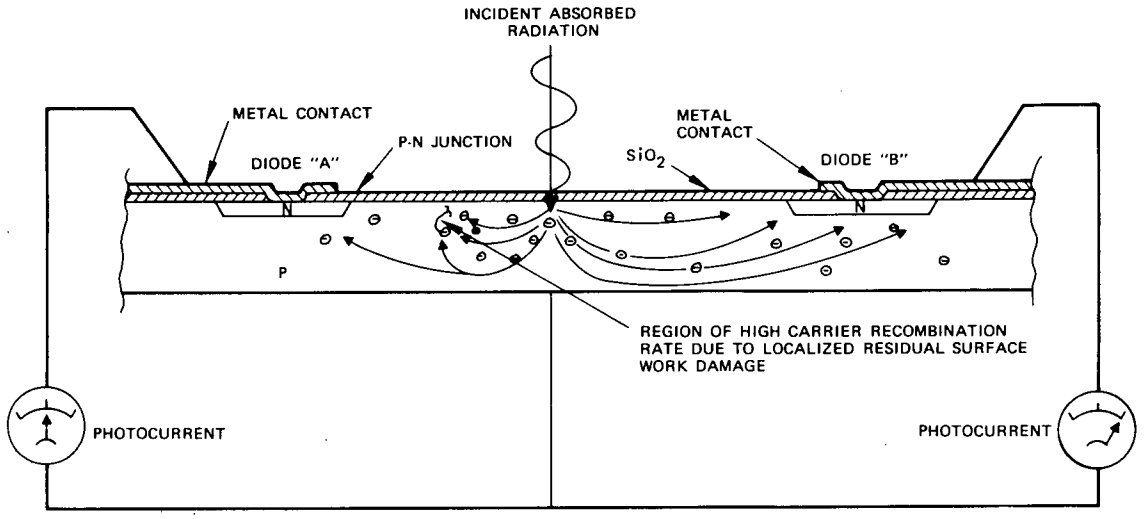

Figure 4. Reduced photovoltaic response of junction due to localized high minority carrier decay rate at work damage site.

These charge carriers move under the influence of applied electric fields and thus act to transport the electrical current in semiconductors. Such photo-generated electrical carriers serve to increase the electrical conductivity of an irradiated sample. A population of such carriers produced by a light pulse recombine eventually and exhibit a "lifetime" which is determined by the structural defect type and density within the crystal lattice. The presence of lattice vacancies, dislocations, impurities (particularly those which introduce mid-levels in the semiconductor energy gap) as well as other crystal structural imperfections, will act as "lifetime-reducing" combination centers at which carriers will meet and recombine. In the case of "indirect" band gap semiconductors (e.g., silicon), the energy required to produce a carrier pair, that is the band gap quantum energy, is liberated upon recombination as thermal energy which serves to "heat up" the crystal. In the so-called "direct" bandgap semiconductors (e.g., GaAs) the lattice is not involved in the recombination. The carriers recombine in this case with emission of radiant energy corresponding to the band gap energy. This is the process which occurs in a light emitting diode (LED). Energy is not transferred by momentum exchange to the lattice during carrier recombination in the direct bandgap semiconductor. Since silicon constitutes the material from

which the great majority of the semiconductor devices of interest to this study are fabricated, radiative carrier recombination processes will not be further treated in this work.

Electromagnetic radiation interaction with semiconductor devices is merely one part of a general area of radiation damage in solids. Radiation damage resulting from high energy particles as well as the entire range of the electromagnetic radiation spectrum has provided a great deal of information and theoretical understanding about the solid state. Various radiation effects are produced in solids such as lattice displacements, chemical changes and transient ionization effects. It is important to understand these phenomena both in a qualitative and quantitative manner, in order to develop a radiation technique for complete inspection of semiconductor devices. Some radiation effects are rather permanent whereas others recover to essentially the pre-radiated state in a short time period. Since it is essential that the technique used for 100 percent inspection should not degrade the device, review of radiation damage in solids has been incorporated in this study. After completing the review of general radiation damage, it appeared reasonable to restrict the attention of this program of work to that portion of the electromagnetic spectrum that may be considered nondestructive.

It should be pointed out that low energy (~100 keV) electron probe techniques, although not included under the electromagnetic heading of this study, should not be discounted for future consideration since many effects of electromagnetic and low energy electron interaction with solids are quite similar. It is not the intent of this study to prejudice the reader against electron probe techniques as generally applied in the Scanning Electron Microscope (SEM) since certain advantages exist in the use of generalized electron probe techniques. A separate study of the SEM technique for 100 percent qualification of microelectronic chips might be advocated.

It is also necessary when considering certain frequencies of the electromagnetic radiation spectrum, to point out that effects other than ionization for production of carriers, may be very useful in contributing to the characterization of devices. In particular, in the case of x-rays, a very useful visualization technique (x-ray topograph) may be used to monitor early

process steps of entire semiconductor wafers by mapping damaged regions of the wafer which have been shown to contain various carrier trapping/ recombination centers within the semiconductor. A brief review of this technique is presented indicating how the x-ray diffraction (Lang) technique may be usefully coupled with the nondestructive electromagnetic technique of the form herein proposed for a more complete qualification of devices.

It is very important to maintain awareness of an optical scanning microscope comparison technique (Automatic Visual Scanning Inspection System, AVIS) which gives visual information about the topography of the device. It is possible that some major elements of that system may be applicable to the techniques reviewed in this study.

4.2 X-Radiation Effects

X-rays interact with solids in several ways. Some of the incident x-rays are scattered and some are absorbed in ionization processes. X-rays lose energy to the electrons in atoms by the photoelectric process. The cross-section for absorption varies with the energy, which implies that inner shell electrons are preferably removed by high energy (short wavelength) x-rays and adjacent outer shell electrons are removed by successively longer wave length x-rays. The wavelength of x-rays extends from approximately 0.1Å to 100 Å.

An important aspect of x-ray interaction with matter, specifically in this case semiconductor material, is the stopping power or range of the material. Characteristic x-rays of wavelength between 0.5Å and 2Å will have an e^{-1} thickness of 250 microns to 5 microns. The variation in range is a strong function of both wavelength and material atomic number. As a consequence, a small part of the x-rays are absorbed by a photoelectric process in the region of interest in a semiconductor device. Higher energy or shorter wavelength x-rays are even more penetrating. The preceding discussion is a way of saying that the semiconductor is quite transparent to conveniently generated x-rays.

The relative transparency does not preclude the photoelectric event from taking place in the vicinity of a p-n junction, and when such an event does occur the number of charge carriers produced is very large. The

initially ejected photo-electron contains essentially a kinetic energy equal to the energy of the incoming x-ray photon. The range for the photo electron is very short and it loses its energy also by the photoelectric process in a region very close to the initial photon absorption event. As a consequence, a 10, 000 volt x-ray photon will produce nearly several thousand hole pairs in a very localized region. The resultant perturbation electrical pulse will be generally very difficult to interpret.

The x-rays will be scattered as well as absorbed in the semiconductor device, however, the wavelength is such that defects such as pinholes, scratches etc. will not greatly affect the efficiency of the photoelectric process. Such defects will be very transparent and virtually unnoticed. In addition to incoherent x-ray scattering, which has just been considered, a crystalline semiconductor material will scatter x-rays coherently, however, not in a manner to produce charge carriers. This useful effect which results in topographic information is considered next.

In general the process of creating hole-electron pairs in semiconductors by x-rays is a rather inefficient one compared to other types of electromagnetic radiation. This would not constitute reason to discount x-rays for the present application of producing an input signal at various points in a semiconductor device and measuring the effect on an electrical output, as presently planned. It is a more important fact that x-rays are not conveniently focused in a manner which would permit rather rapid x-ray scanning while synchronously observing electrical output signals. In fact electromagnetic radiation of wavelengths less than 1, 000Å is not amenable to live focusing and is therefore very difficult to handle. Before leaving the x-ray region of the spectrum, it should be noted that x-rays have wavelengths of the same order as the interatomic spacings in a solid and, therefore, can be coherently scattered in discrete directions as governed by the Bragg equation:

$$n\lambda = 2d \sin\theta$$

where λ = x-ray wavelength, d = lattice spacing and θ = angle of incidence of x-rays upon a set of parallel planes.

Wafers from which semiconductors are made are essentially slices of large single crystals. Therefore a proper orientation of a semiconductor wafer in a well collimated x-ray beam, can result in a photographic map (topograph) of the wafer in the manner of Lang. Regions of lattice damage do not satisfy the Bragg equation as do the adjacent perfect regions. Scanning a properly oriented wafer past a narrow slit of x-rays results in strong diffraction of the x-rays where the wafer is perfect and a much stronger scattering where the lattice is distorted due to reduced extinction effects. A recording film which moves simultaneously with the wafer provides a record in direct correspondence with the wafer.

It is well established that damaged regions provide recombination or trapping centers for carriers in semiconductors. This adversely affects one of the most important device-determining solid state parameters, the carrier lifetime. Damage due to mishandling by tweezers or in furnace boats, etc. may be detected at various early stages of the wafer processing. It might be asked why the Lang technique has not been more widely used for screening wafers if such good correlation between performance and Lang topographs exists. Firstly, fairly elaborate equipment with skilled operators is required and secondly a rather long time (approximately 8 hours) was required for application of the original Lang technique to a given wafer. The long time scan results from wafer warpage during processing. Schwuttke devised an oscillating specimen holder which reduced the time considerably (SOT technique); however the oscillation technique still does not obviate the fact that the Bragg angle is only satisfied for a small fraction of the oscillation cycle. More recently a feedback loop from the scattered signal has been utilized to maintain the sample in the proper Bragg orientation at all times, thus reducing the scanning time greatly. Further utilization of this technique may be expected, although the x-ray diffraction technique does not obviate the need to perform final device testing since process variables and accidents can still affect the device in the later processing steps.

It should be pointed out that impurity precipitates which create strain fields and therefore local lattice rotations may often be detected by this technique. A correlation observation of oxide pinholes employing visual and

scanning electron microscopy might well provide a non-destructive screen for these very troublesome defects which can act to reduce device reliability.

4.3 Optical Radiation Effects

Electromagnetic radiation (photons) in the ultraviolet, (2000-4000Å), visible, (4000-8000Å) and infrared (8000Å and up) incident on a semiconductor, generates one or more hole-electron pairs per absorbed photon, which increases the conductivity of the material. Semiconductor bulk and surface anomalies will affect the hole-electron pair generation efficiency as well as the decay rate of the generated pairs. In the field existing at a zero or reverse biased p-n junction in the semiconductor, these generated hole-electron pairs are separated leading to the development of a junction photo voltage. In an operating semiconductor device this photo-voltage or some derivative of it will appear at the terminals of the device, thus modifying the electrical signals generated there.

The following mechanisms serve to modify the light entering the semiconductor which in turn reduces the resultant photovoltage:

- Absorption
- Reflection
- Interference
- Scattering

Types of defects in the semiconductor device structure due to material and process errors which will cause modification of the incident light associated with the semiconductor device, are the following:

1. Pin holes in oxides
2. Impurities in or under the thermal oxide
3. Contamination in or under the passivation layer
4. Passivation thickness and porosity (density)
5. Masking flaws
6. Metallization defects

For example, the presence of a pin hole in the oxide layer could act as a light scattering center depending upon the size of the pin hole and the wavelength of light. Light scattered from a specific region at a pinhole will

not be available for pair generation and thus, will reduce the effect sensed at the electrical output terminals of the device. Oxide pinholes are of two general types:

1. Mask generated (dust, scratches, etc.).
2. Bulk defect generated (dislocations, etc.).

Pinholes of the first type will occur without any disturbance of the underlying semiconductor. Light impinging upon such pinholes will merely be scattered, thus reducing the population of photo generated carriers and hence the photo response intensity in the immediately adjacent semiconductor as described above. Pinholes of the second variety will, in addition, have bulk crystal structural defects (dislocation, etc.) associated with them. These defects will reduce the lifetime and hence the decay characteristics of the photogenerated carrier population.

Differentiation between these two types of oxide pinhole defects becomes one of measuring intensity vs lifetime effects of photo-generated carrier populations in localized affected regions of the device surface.

A second set of phenomena associated with the fate of photo-generated hole-electron carrier population within the semiconductor crystal requires discussion. In the "perfect" semiconductor the generated hole-electron pairs will eventually recombine. In a real semiconductor device however the rate of recombination will be enhanced due to the presence of defects. Defects may be either structural (vacancies, dislocation and interstitials) or impurities (such as substitutional dopants). Manufacturing errors such as scratches, cracks and residual work damage with associated contamination will enhance carrier recombination rate by generating structural crystal defects and impurity centers of the above types.

A population of hole-electron pairs generated by a pulse of light experiences a decay rate which will be determined by the existence of these types of structural defects in the device crystal structure. A convenient way of observing the pulse of photo-generated carriers is by means of the photo-voltages developed at p-n junctions contained within the device.

The photo-response of a p-n junction contained within a given device will thus be modified by the presence of the following types of fabrication errors in the junction vicinity:

1. Residual work damage
   a. Scratches
   b. Lapping/polishing errors
2. Mechanical Stress
   a. Thermal shock
   b. Oxide/semiconductor interface thermo-mechanical mismatch
   c. Stress at lead-bond sites due to "overbonding"
   d. Probe testing damage
3. Presence of Midgap (Lifetime reducing) impurities
   a. Gold (Au)
   b. Copper (Cu)
   c. Iron (Fe)

4.4 Radio-Frequency Radiation Effects

The radio frequency spectrum is generally considered to encompass frequencies between 10 KHz and 1000 GHz, with corresponding approximate wavelengths of 3×10^4 meters and 0.3 mm. Practical use of the upper frequency end of the spectrum is limited by available signal sources and apparatus to frequencies below 300 GHz ($\lambda \geq 1$ mm).

This portion of the electromagnetic spectrum presents two significant limitations when applied to semiconductor screening, lack of quantum energy and poor dimensional resolution.

The energy limitation becomes evident when one calculates the quantum energy for wavelengths at the high frequency ("best case") end of the RF spectrum (e.g., ~1 mm or ~1000 microns). The photon energy corresponding to this order of wavelength is in the range of ~0.001 eV. This is sufficiently far below the band gap energy in silicon (e.g., 1.12 eV) as to be negligible in hole-electron pair generation. The photon equivalent of kT at room temperature (0.025 eV) is itself far in excess of that for RF quanta.

With reference to resolution, the long wavelengths of even the highest frequency RF radiation (1000μ) sets a resolution limit well below that required to detect defects of the order of size encountered in microelectronic structures (e.g., 1 - 10μ).

Although measurements of bulk resistivity by means of coupling with a microwave RF field have been done with large pieces of raw semiconductor material (ingots and large wafers), the applicability to small samples (e.g., chips) is of limited feasibility and usefulness in this study.

For these fundamental reasons, as well as the lack of evidence in the relevant literature of useful applications for RF in measurement of semiconductor material properties and defects, this region of the electromagnetic spectrum offers little potential as a means to excite semiconductor devices.

4.5 Electromagnetic Pulse Effects

Considerable interest exists in the phenomena of "Electromagnetic Pulse" (EMP) effects under the category of radiation interactions with semiconductors and other components. Within the context of this report, such effects are not due to direct interaction of electromagnetic radiation with the active device element itself. The passing electromagnetic wave train is reduced to a purely electrical pulse through "antenna pickup" by associated wiring and interconnections. It is this purely electrical pulse which is delivered to the device through metal contacts, etc. which produces degradative changes in some devices. Such effects are therefore not electromagnetic radiation effects and hence fall outside of the scope of this report.

5.0 ELECTRICAL SIGNALS AND THEIR ANALYSIS

The electrical signals obtained from electromagnetically excited semiconductors will generally be very complex, particularly those from integrated circuits. The analysis and interpretation of these signals constitutes a major task in the development of an electromagnetic screening process. Two techniques offer means to considerably simplify the signal analysis task, scanning of the exciting radiation and utilization of a reference standard device for comparison.

5.1 Scanning the Excitation

Scanning of the exciting radiation to locally irradiate the device with a moving spot provides considerable simplification of the output signal by limiting the response at a given instant to a small portion of the chip. By using a repeating scan or raster the position of the spot can be correlated with time to essentially add another dimension to the output signal.

The advantages of scanning are obtained at the expense of a more complex irradiation system. However, this may be more than offset by the simplification of the signal processing task and equipment. A further criticism of the scanning approach is the difficulty of operating at x-ray wavelengths. The scanning approach is essentially limited to optical radiation.

5.2 Reference Chip Approach

The second signal simplifying method using a reference device for comparison has no wavelength restrictions and is applicable to both the scanning and non-scanning (flooding) techniques. Basically, the method uses a "perfect" reference device that is synchronously exposed to the same

radiation as the test device to provide an "ideal" set of electrical signals. By subtracting these ideal outputs from the equivalent test device outputs, resultant signals representative of the differences between devices are obtained. These differential signals can be analyzed more easily than the direct output signals to provide "fingerprints" of device flaws. These fingerprints may not be readily identified with specific defects, however they should be indicators that one or more defects exists in the test device.

The basis of the differential signal is the photocurrent (electron-hole pairs) generated by p-n junctions within the semiconductor material. These photocurrents are determined by the number and energy of the photons which reach the material. However, such photocurrents are reduced by recombination and trapping processes within the device. In addition, the amount of radiation (photon flux density) which reaches the active semiconductor volume will have been reduced to some degree by the various physical processes of absorption, reflection, interference and scattering occurring prior to its absorption by the semiconductor to produce carrier pairs.

Typical defects in the semiconductor device which will cause a modification in the intensity of the incoming radiation, by one or more of these mechanisms are:

1. Pin holes in oxide
2. Impurities in the oxide
3. Passivation thickness and density
4. Contamination under the passivation layer
5. Masking flaws
6. Metallization defects

To detect the small effect these defects have on output signals, it is essential to remove other sources of difference signals between two chips. Typically, edge effects due to both masking errors and misregistry between the two chips must be removed.

When the chips are equally excited by flooding, the major signal differences will be the result of fundamental differences between chips with little opportunity or need for adjustments other than signal amplitude.

However, when radiation scanning is used, the system is sensitive to differences in chip size, position, orientation, and minor masking deviations. The elimination of difference signals from these causes will be a major task in the implementation of a screening system of the scanning type. Computerized control of chip alignment and registration will likely be necessary to attain a system suitable for production usage. Some details regarding the implementation of an alignment and registry system are covered elsewhere in this report.

A complete discussion of fingerprint utilization presumes successful registration of the chips. Because the registry may be accomplished only within certain narrow limits, the remainder of the edge effect difference can be ascribed to masking errors and poorly defined edges.

1. Pin Holes in the Oxide

   In an otherwise transparent oxide, pinholes of the order of the radiation wavelength and larger will scatter the radiation and reduce the amount which reaches the active semiconductor region. If the reduction in the number of photo-induced charge carriers can be electrically resolved they will provide a fingerprint of oxide pinholes.

2. Impurities in the Oxide

   Impurities in the oxide can act as highly absorbing regions or as scattering regions for the incident radiation. In either case, the intensity of the radiation and thus the photo-current is reduced. Localized impurities would thus have the same general effect as pinholes, on the photo-current, whereas a non-localized distribution would reduce the photo-current rather uniformly over a larger area.

3. Passivation Layer Thickness or Density Change

   Depending upon the direction and magnitude of the thickness/density change, the photo-current will be changed accordingly. Surface roughness will also affect the amount of radiation transmitted and appear as "noise" in the displayed signature. Other defects which are of greater interest however, should still generally be detectable against this background.

4. Impurities at the Passivation/Semiconductor Interface

   In addition to scattering and absorbing processes by impurities in the glass, charging of impurity atoms at or near the passivation/semiconductor interface may alter the semiconductor by inverting its conductivity type from n- to p- or vice versa. The electrical effect due to carrier lifetime changes would produce an identifiable fingerprint of the defect.

5. Masking Errors

Masking errors will appear as part of the general edge effect signals, viz, lack of registry with reference chip, masking errors and etching mistakes. Those edge effects which exceed the inherent uncertainty in registration between the two chips may be identified as masking or etching errors.

6. Recombination and Trapping Centers

The previous group of defects residing outside of the active semiconductor regions of the device not only affect the amount of photoelectric current by altering the number of photons which reach junction regions, but they may, along with other defects in the semiconductor, exert a perturbing effect on the charge carrier lifetimes. These perturbations contribute significantly to the detailed structure of the fingerprint or signature of the device.

The fate of the charge carrier induced by the radiation source will depend upon defects present within the semiconductor since the rate of recombination will be enhanced due to the presence of defects. Lifetime affecting defects may either be structural (vacancies, dislocations and interstitials) or impurities (such as substantial dopants). Manufacturing errors such as scratches, cracks or residual work damage will increase recombination rate by generating structural defects of these types.

A population of hole-electron pairs generated by a pulse of radiation experiences a decay rate which will be determined by the number and kind of recombination centers in the device crystal structure. A convenient way to monitor the pulse of photogenerated carriers is by means of the photo-voltage developed on the p-n junction contained within the device. The photo-response will thus be modified by the presence of various fabrication errors in the junction vicinity.

5.3 Device Signature

The signature which is obtained as a result of subtracting the photoelectrical response of the reference chip from that of the unknown chip, constitutes a large assemblage of information, not all of which is necessarily relevant to the problem of identifying flaws in the unknown device. Flaws are defined here as defects which compromise the electrical performance and long term reliability of a device. A fundamental requirement in developing a screening system is the development of techniques which eliminate from the displayed signature of a given device, those details of structure which are not meaningful. The use of the reference chip itself constitutes a

major step in this direction by cancelling out those basic designs and structural details which are common to all devices of the sort under examination. The reference chip which serves to cancel out this large block of useless information does not, however, remove from the signature uninteresting and irrelevant information. For example, the sequential mask alignments employed in fabricating an integrated circuit are performed within some arbitrary process specification limit of accuracy. Hence, minor misalignments of diffusions and metallizations inevitably occur in any real integrated circuit device. If a scanning excitation system is used, these trivial differences between reference chips and unknown chips will make themselves evident in the resultant signature. This is shown schematically in Figure 5, in which a single line scan response across a pair of slightly misaligned p-n junctions is shown. A structural flaw of significance is included in the overlap region area in one of the windows (unknown device). The response due to the misaligned border is of no significance, whereas the response due to the flaw would be meaningful.

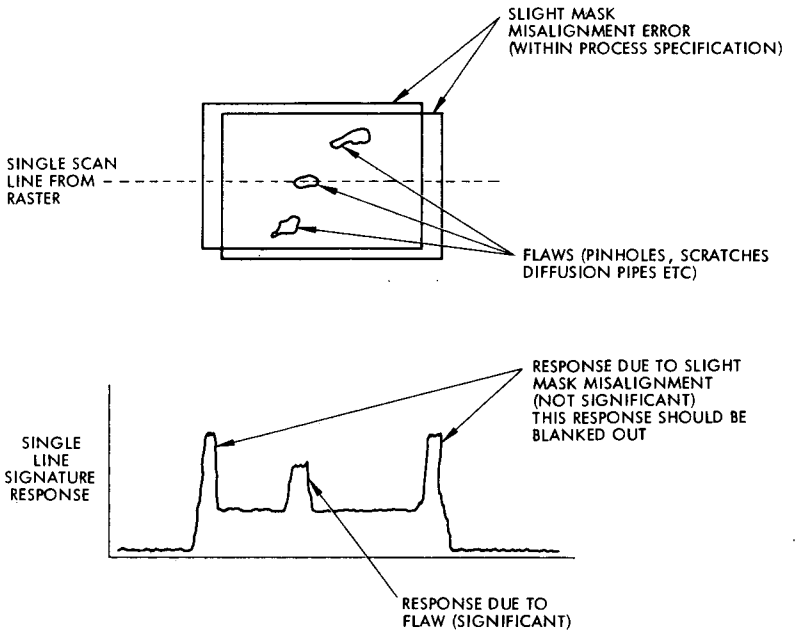

Figure 5. Systematic and non-systematic error display.

The foregoing discussion points out the need for techniques which remove uninteresting information from the signature and thus effectively make it more meaningful. It is quite desirable, that blanking techniques derived from the chip design format be employed to cancel out such trivial information. Thus an improvement in the "signal to noise" ratio in the signature is produced by the use of the reference chip approach itself and programmed blanking techniques of the sort just discussed.

Figure 6 presents a schematic representation of the total information content of a chip evaluated in a scanning system and the manner in which it can be handled to improve the meaningful information content of the resultant signature and hence to simplify its interpretation in terms of device defects.

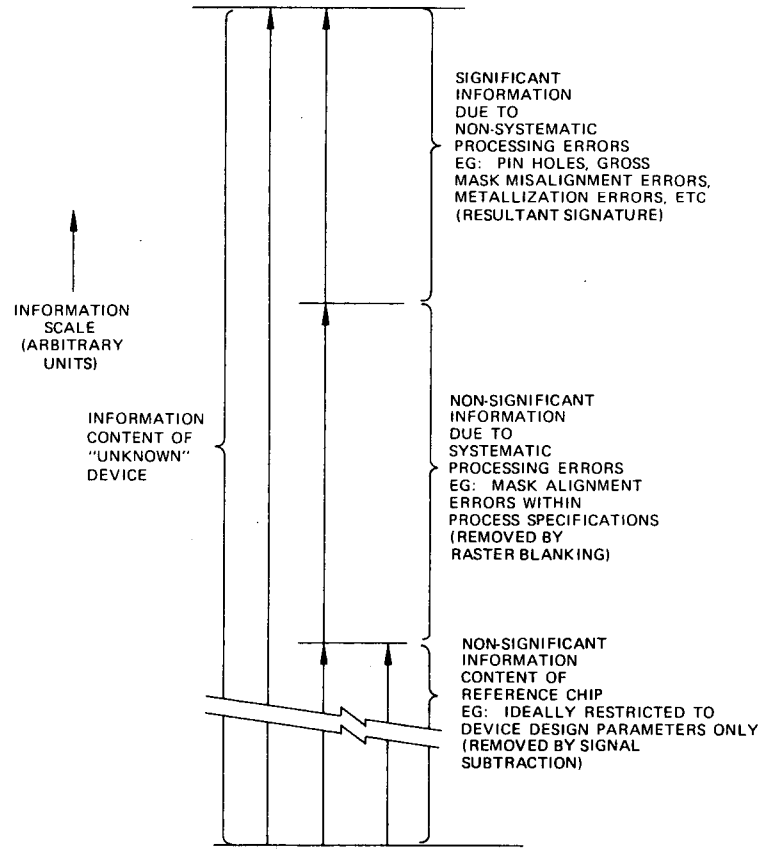

Figure 6. Schematic representation of information content of semiconductor device chip.

The family of signatures obtained for any given device with various lead selections and applied electrical biases will represent a very large assemblage of information. The reference chip approach greatly reduces this volume of information by eliminating that basic block of information contained in the standard design parameters for the device. The "residual" information then will be due to incidental structure differences between the reference and the unknown devices, and includes cumulatively all "errors" in materials processing and fabrication of the unknown device. Not all of these errors are of such a nature as to compromise device performance or reliability, however. These errors may be divided into systematic (non-degrading) and non-systematic (device-degrading) types.

For purposes of discussion here the reference device is assumed to be "perfect." This assumption and its limitations are treated in another portion of this document. This concept is expanded in Figure 6 in which the three basic categories of information are schematically represented in a simplified one dimensional manner. A typical systematic error would include, for example, a minor mask misalignment within process tolerance specifications. Such an error would not produce a device degradation in performance and/or reliability but would generate a response on the scanning system. Such uninteresting response would be dealt with by "blanking" technique as discussed elsewhere in this report.

5.4 Defect Signature Analysis

The manner in which a signature is developed for a typical flaw in an unknown chip is shown in Figure 7. For purposes of simplicity a single line (one dimensional) response is shown. The flaw selected in this case is a channel on a device surface. Channels of this sort may be generated by a number of causes, for example: oxide contamination, electrostatic charging of the oxide, mechanical stress within the oxide, etc.

The response of nearby non-disturbed junctions, the effects of metallization shadowing, etc., are ignored in this simplified schematic. In a real situation, however, these and many other details of the device structure will make their effects known and must be dealt with in real signature interpretation.

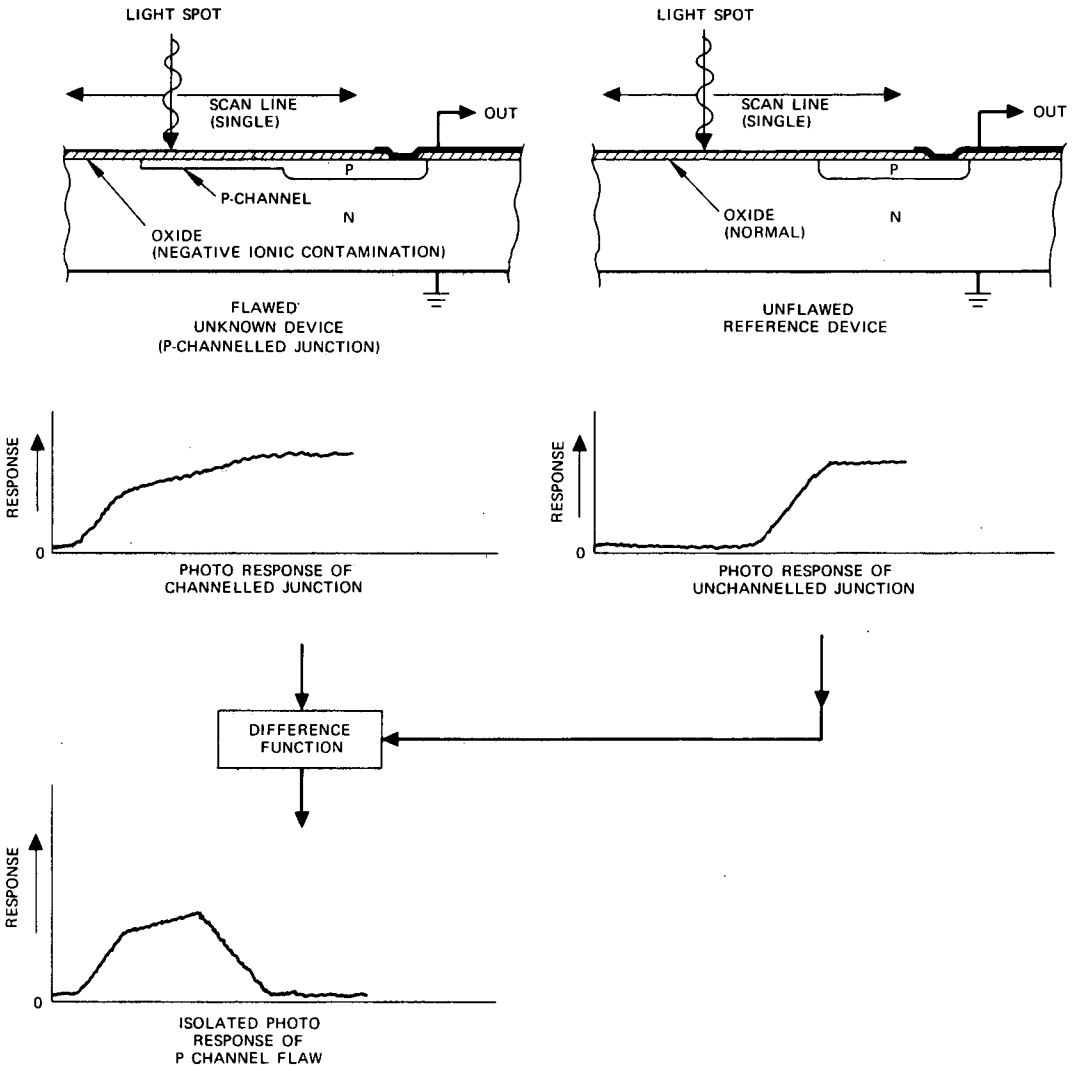

Figure 7. Typical surface channel flaw response.

The responses of the reference chip (no channel) and the response of the unknown chip (with channel) are shown adjacent to each other. It will be observed that a photo-response for the junction in each case is obtained at some distance away from the junction as indicated by the slope of the response curve, as the light spot approaches or retreats from the junction area. This slope is determined by the free carrier lifetime of the semiconductor material. If the disturbance which produces the channel, (e. g. inversion layer) should also produce changes in carrier lifetime the slope would be

appropriately modified. The second reduced slope region corresponding to the channel itself is due to channel sheet resistance. Effects which produce inversion layers introduce energy levels in the energy gap near the conduction band (n-type) or the valence band (p-type) whereas life-time influencing factors introduce midgap levels within the semiconductor. In order to preserve simplicity in this presentation, possible lifetime influences are ignored.

The responses of the reference and unknown devices upon subtraction of the signals will yield the final display of the channel flaw itself exhibited in isolation from other influences. What has been accomplished here, in effect, is an improvement in the output signal by the subtraction of uninteresting information common to both devices. There then remains for interpretation only the isolated response of the device flaw itself.

6.0 IMPLEMENTATION METHODS

The contents of the previous sections have indicated that the optical portion of the electromagnetic spectrum will be the most effective in stimulating signals to reveal semiconductor flaws. This section reviews the task from the viewpoint of implementing an operating inspection system. Both scanning and flooding techniques are reviewed.

6.1 Optical Scanning Approach

Fundamental to the scanning approach is a raster generating system. In developing a raster system, a number of subsystems or components are necessary:

1. The light source (coherent or non-coherent)
2. A light deflection system (oscillating-rotating mirror arrangement)
3. An optical imaging system (lenses, prisms, beam-splitters, collimators, etc.)
4. Light pulsing - modulating technique (mechanical choppers, Kerr or Pockels cells)

Considering the above optical system variables, it appears that in the interest of technical ease of implementation and ultimately in terms of cost that a laser is the optimum light source. This conclusion is based on the following factors:

1. The high degree of collimation already existing in the laser beam simplifies the optical system required as compared with the lens system which would be needed with a non-coherent light source.
2. A non-coherent light source, e.g., a gas discharge tube, would require the use of an expensive and sophisticated optical monochromator in order to obtain monochromatic light. No such monochromator is required with a laser light source.

3. The need for pulsing, modulating, and blanking the light source would pose considerable difficulties with a non-coherent gas discharge light source. This is not so with a laser device. A continuous laser light source may be pulsed or otherwise modulated employing purely electrical techniques, thus eliminating the need for expensive opto-mechanical or opto-electronic ancillary equipment.

Laser Scanning Techniques

A possible scanning laser system is presented schematically in Figures 8 and 9. The optical portion of the approach comprises the functional heart of the system. A laser capable of operating at two levels of power is the source of the radiation for generating the final raster display (low-power mode) and of exciting the device(s) under study in accordance with some desired optional program (high-power mode). A second laser probe which may be positioned at a single corresponding location on the two devices is provided in order to allow continuous excitation of a given device element independent of the primary excitation raster.

The radiation from the primary laser passes through an optomechanical raster generator consisting of two moving mirrors. The first mirror oscillates at a desired raster frame rate frequency, (e.g. 20.0 frames per second.) The second mirror rotates at a frequency which is set by the desired raster line rate. A precision multi-faceted mirror is used for this purpose. Both the oscillating and rotating mirror rates are set and synchronized by the generator employed to produce the CRT display raster shown in Figure 9.

The rasterized laser beam is then reflected by a succession of two fixed mirrors into a single eyepiece of each of two conventional binocular microscope heads. The auxiliary non-rastered laser is introduced into the optical train by means of a third fixed mirror. The first of these mirrors is semi-reflecting in order to allow the remaining fraction (approximately half) of the signal energy to enter the corresponding eyepiece of the second binocular microscope.

The two microscope heads then image the laser beam raster onto each of two nominally identical semiconductor chips mounted on the stages of the respective microscopes. The chip under evaluation and the reference chip are designated Chip "A" and Chip "B" respectively.

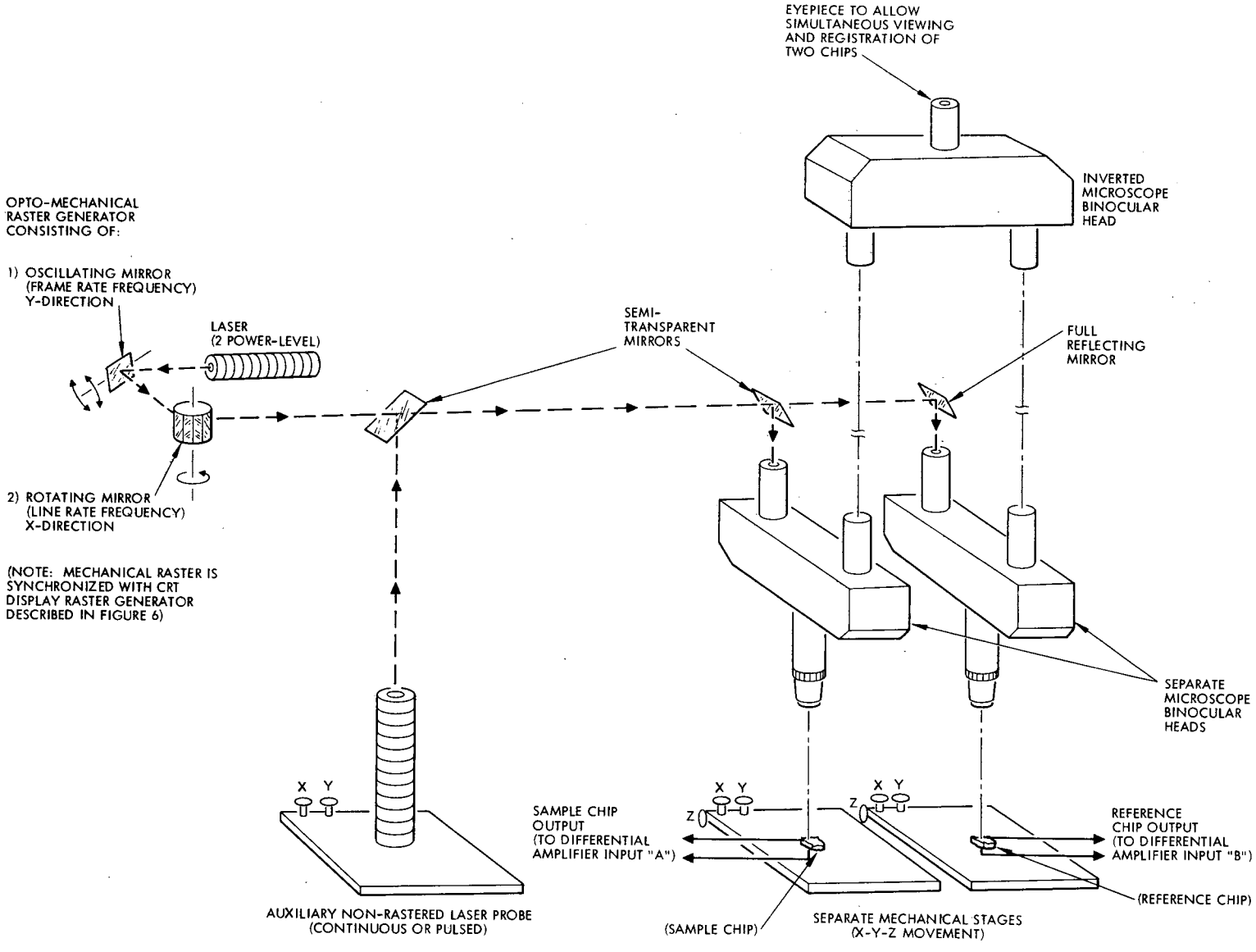

Figure 8. Opto-mechanical arrangement for the laser scanning system.

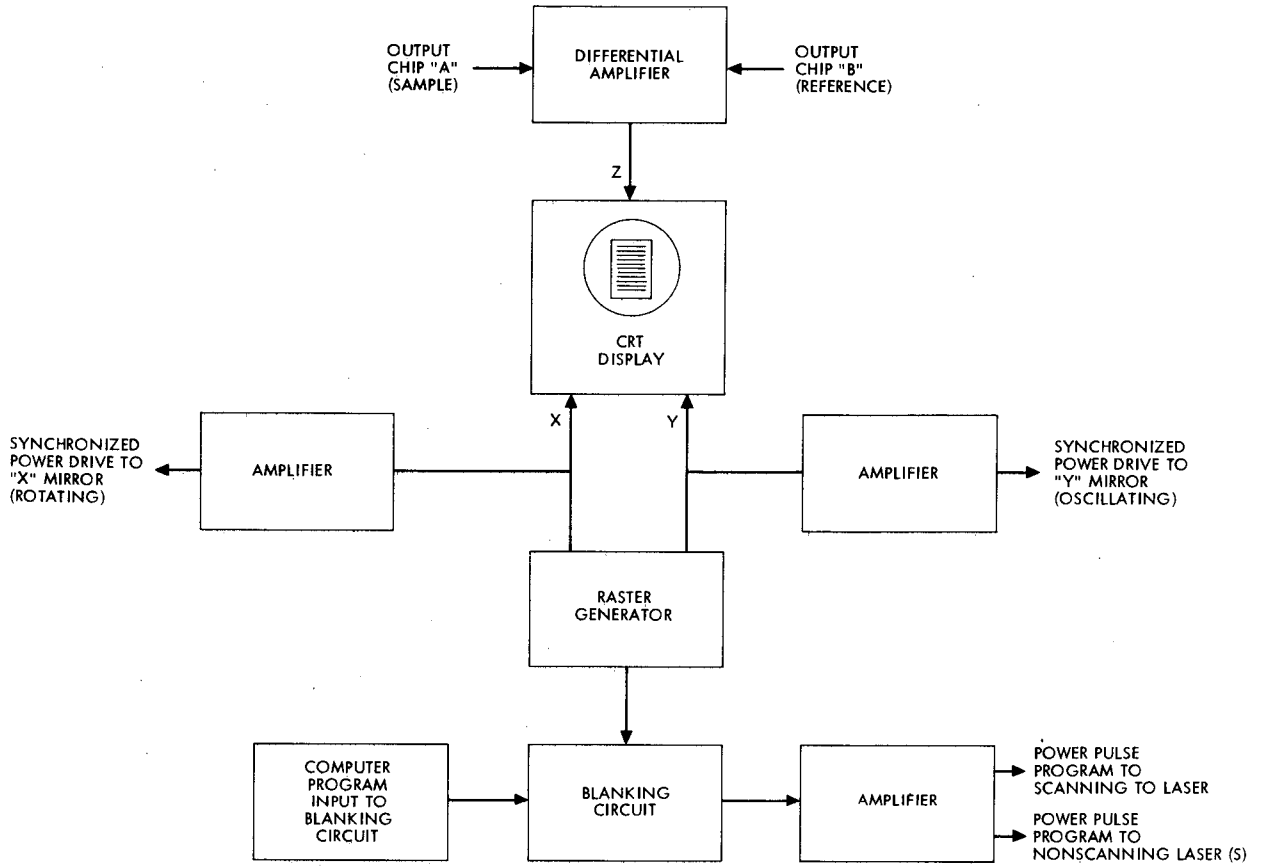

Figure 9. Block diagram of electronics and display of a laser scanning system.

In order to observe both chips simultaneously, a third binocular microscope head is mounted upside down on the two remaining eyepieces of the first two microscope heads, as shown in Figure 8. The inverted microscope is provided with an eyepiece positioned where the objective lens would normally be located. Registration and focusing of the two nominally identical chips is accomplished by means of this eyepiece, employing the x-y-z and small angle polar movements on the respective microscope stages.

An output from the two chips is provided by two pairs of leads connected to the same two corresponding sets of leads from the two devices. This arbitrary lead selection is determined by the particular circuit configuration under consideration and may be selected from a large number of permutations and combinations possible with a multileaded device. The two

signals developed by the two devices are then processed through the differential amplifier shown in Figure 9. The differential amplifier output is then employed to intensity-modulate the raster on the CRT display tube. In the improbable ideal case in which Chips A and B are precisely identical, the output of the differential amplifier will be zero for all corresponding points on the chip surfaces. However, in actual real cases the two chips will not be identical and will differ in detail due to variations in their history and consequent structure.

Pulsed and Auxiliary Laser Excitation Mode

It is desirable to have the capability for pulsing the laser to an enhanced output power level (i. e., 10X) during the raster period, according to any desired prearranged program. This allows simultaneous excitation of corresponding points on two test devices in any desired pattern. This pattern could correspond to the location of specific circuit or device elements of interest. Thus, certain elements not accessible electrically through external terminations may be exercised to provide a degree of dynamic evaluation of the device. The second laser provides this capability continuously or in a pulsed manner, independently of the raster frame-line rate.

Optical-Mechanical Aspects

To use the fingerprint concept, it is desirable to simultaneously irradiate and electrically examine equivalent regions of the reference and test chips. An optical system may be devised from existing technology utilizing a beam splitting process which will provide two small spot-size beams of identical intensity. It is also possible to see the two illuminated regions with the same optical system. It is then only necessary to orient one chip with respect to the other in such a manner that they superimpose optically to the extent that both chip images are coincident.

The precision with which two chips can be mechanically placed in registration is determined by the system optics; however, this is not the laser precision limit of registration. After relatively coarse optical alignment, an electrical difference signal from suitable alignment regions can be adjusted to a minimum, thus producing the best achievable overlay of the two chip images.

The edge effects from non-overlay which persist was discussed previously as part of the fingerprint concept. In order to achieve rapid, precise, automatic registration it is necessary to interface the differential output signal employing a computer and also to interface the positional controls with a computer. The computer will seek a minimum differential signal by moving the reference chip in the proper directions.

The mechanical stage which holds one of the chips must be movable in X, Y and Z directions and rotatable about a vertical axis. All of these motions may be electrically controlled by the use of electrical stepping motors for coarse motions over large distances and electrically activated piezoelectric motion for fine motions over small distances. Computers such as the PDP-8 with easily developed programs have been used in similar applications for several years.

6.2 Optical Flooding Approach

The technical complexity and the associated costs involved in developing the scanning excitation approach suggests that a simplified preliminary study in which a non-scanning flooding approach could yield valuable practical results on a much reduced time-cost schedule. Some technical information as to behavior of flawed devices which will be relevant to the subsequent implementation of the scanning approach would thus be obtained.

The previously described spot scanning approach is one of considerable technical intricacy. Consequently, although the scanning approach is highly desirable in relation to its ability to resolve and detect semiconductor device flaws and the simplification of signal processing, it involves certain difficult technical problems. Among these are the following:

1. Image alignment of reference chip and unknown chip. This critical requirement involves complex and costly opto-mechanical fixturing.
2. The complex blanking functions to be performed by the associated computer will require a significant software programming package for each device under consideration.
3. The scanning approach will generate a very large volume of information relative to any particular device chip under consideration. Not all of this information will be relevant or necessary

for the simple go-no-go acceptance/rejection requirement for inspection in production. Some of the information generated is more related to identification of the specific failure mechanisms in failure analysis rather than to production inspection functions.

In view of the above considerations, it is recommended therefore that a preliminary investigation of the effect of radiation flooding upon device electrical behavior be undertaken to assess its merit relative to production inspection. This recommendation does not constitute a departure from the ultimate objective of development of a flying spot scanning inspection technique, but is rather a technical preliminary to that endeavor. It is felt that considerable information with regard to a given device's photoelectrical response may be obtained in such an experimental program employing techniques of a simpler nature and a significantly lower cost.

Effects of Flaws on Device Photo Response with Irradiation Flooding Mode

The presence of a flaw in a device structure will, if it is sufficiently severe and strategically located near an active region of a device, produce a variation in electrical characteristics of that device as previously discussed. Thus an abrasive scratch in the semiconductor surface, residual work damage or a contamination generated surface channel, for example, will act to degrade junction reverse leakage, capacitance and reverse breakdown. All such device degradation will presumably be detected in conventional device electrical testing under dark conditions.

In some instances, however, a flaw may exist in the device which does <u>not</u> change dark electrical characteristics but <u>can</u> modify the photoresponse of the device. The existence of a device structural defect which scatters, reflects or absorbs radiation on one hand or modifies photogenerated electrical carrier density and lifetime on the other, can cause a change in device photo-electrical response. Such flaws may or may not be related to device reliability, but they do certainly represent a "deviation from the norm". Conservatively, therefore, in the interest of improving reliability by removing "mavericks", the rejection of such devices may be meritorious and could justify the application of a radiation flooding selection technique to production pre-cap inspection.

Limitations of Flooding Methods

The fundamental physics involved in applying the flooding approach to detect semiconductor flaws is not in principle different from that already presented relative to the spot scanning technique previously discussed. Consequently, only those aspects of flooding approach in which a significant difference from the scanning technique exists will be considered here.

There are, however, certain limitations which might be expected in flaw-detection ability of the flooding technique as compared with the scanning approach. The flooding technique will be inherently less sensitive to flaw detection as compared with the scanning approach. This arises out of the fact that with flooding, the photo response of the entire device is observed simultaneously at any point in time and the effect of a flaw will be observed against a large background of photo-response information coming from many other portions of the device structure.

Employing the scanning approach, however, at any instant in time only a portion of the device corresponding to the spot size will be interrogated and the photo response effect of a given flaw will thus be greatly enhanced. Less critical flaws will thus be detectable. The ability to detect a flaw of any given size or electrical effect will thus be reduced to some degree employing the flooding approach.

As indicated above, some improvement in flaw detection ability over what might be possible employing purely electrical testing may be realized using flooding. In addition some necessary preliminary insight into the photo-electronic effects of device flaws applicable and preliminary to the development of the scanning technique may be obtained in such a study by employing the relatively simple and low cost flooding instrumentation.

X-radiation Flooding Approach

In the discussion of the scanning techniques, the use of x-radiation was excluded due to difficulties in focusing necessary to produce a well defined spot for scanning purposes. In the flooding approach such a limitation of course does not exist and therefore x-radiation may be employed with some possible advantages. Principal among these is the fact that metallization may be penetrated with x-rays to detect possible flaws in regions which

might be "shaded" to ordinary light or impaired radiation. Due to the large "quantum yield" of photo-produced carriers by high energy x-ray photons, simple interpretation of results will be difficult as discussed previously. An additional negative factor in the use of x-rays in production is of course the radiation hazard to personnel.

Experimental Considerations

Use of the flooding technique can best be implemented using the reference chip concept discussed previously in relation to the scanning approach. A possible experiment arrangement is shown in Figure 10.

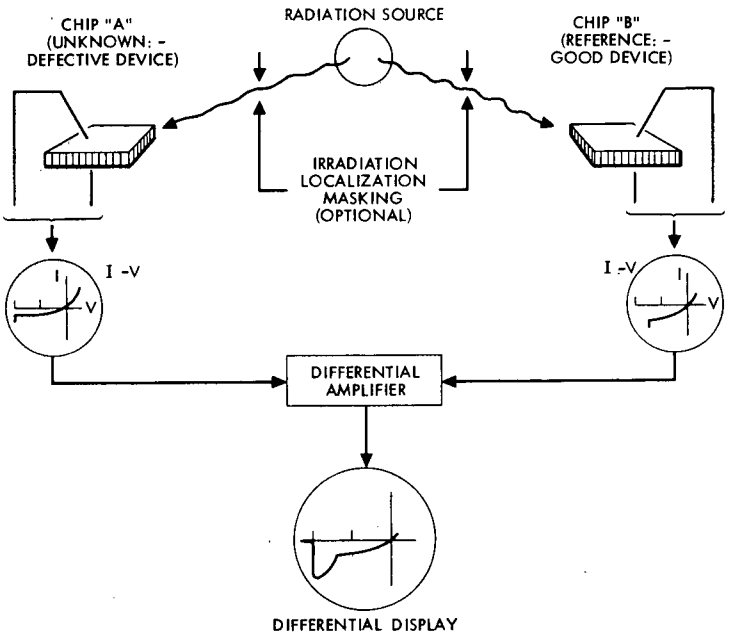

Figure 10. Differential display for reference (good) versus unknown (defective) chip employing flooding excitation (For I-V plot case)

In the case shown in Figure 10, the I-V characteristic of the reference device is subtracted from that of the unknown device to produce a differential display. The display produces a signature or fingerprint for the unknown device which will be characteristic of the flaw generated degration.

This final display represents only the difference between the two devices free of all spurious information due to the "normal" characteristic of the device type under observation. This idea is identical to that discussed previously in this report under "reference chip approach" for the scanning instrument case. In the illustration in Figure 10, the I-V plot differential is presented. Similar displays for a C-V or a device response time difference plot may be generated under irradiated conditions. Presumably, no differential signature will exist for "good" devices which have been previously qualified by ordinary electrical test in the dark.

In the case presented in Figure 10, the differential signal originates due to a device flaw which causes photo generated carriers to recombine in the "flawed" device thus contributing less to its photo response current than is observed for the "perfect" reference device. In effect the photo response of the reference device is greater than that of the flawed unknown device due to carrier recombination at the site of the flaw. Of course, from this display, no information may be derived as to the size, shape or location of the flaw. However, this limitation of flooding does not preclude its application to production inspection for "maverick" devices.

Localized Flooding Modification

The device under examination may be locally excited by the use of masks which restrict the flooding only to specific regions on the device chip surface of greatest interest. This modification begins to introduce some of the difficulties of "registration" discussed previously under the scanning approach. However, if the localized region is sufficiently large such problems may remain trivial and considerable additional information as to the approximate site location for the offending device flaw may thus be obtained. This modification is indicated schematically in Figure 10 as an "optional localized masking".

7.0 APPLICATION OF THE COMPUTER TO A RADIATION SCREENING SYSTEM

The ultimate objective is the application of an electromagnetic excitation system as an automatic inspection system to detect visible as well as non-visible defects in microelectronics devices by their effects on photo excited electrical output measurements.

It would be possible to establish a "signature" or "fingerprint" electrical signal from a semiconductor device without utilizing the reference device concept noted in the previous section. However, by employing the reference device we are applying the principle of small differences between large numbers as a means of improving the instrument sensitivity and to simplify flaw detection.

7.1 Signal Processing

To make such a system automatic, it is desirable to incorporate a computer to act upon the difference signal, recognize the signal and properly identify it as if it were a unique fingerprint of the unknown device.

The fingerprint as first received by the computer may be somewhat "smudged," however further electrical image improvement may be implemented by the computer in such a manner as to clarify the fingerprint and thus render it more meaningful in terms of device processing flaws.

Although it is within the realm of computer technology to perform a complete analysis of all electrical signals from a single device, the current approach toward a simplified technique would require the computer only to analyze the data more completely when a "flag" which consists of a suitably large difference signal is raised. Comparison of two identical devices would result in no flags being raised. In that case the computer would be programmed to accept the device. The obvious advantages of the reference

comparison technique is signal simplification. No extraneous data due to device "normal" structures would thus be processed.

To implement the computer program it will be necessary to establish the magnitude of the differential signal which constitutes raising a warning flag. Considerable knowledge of semiconductor device physics will be required to analyze properly the differential signal as well as the absolute signals. However, even without completely understanding, the exact nature of the observed fingerprint differences, it should be possible to establish go-no-go selection criteria which correlate with device performance and reliability.

7.2 Electrical Excitation Program for Device

For any given device under observation, the complexity of the signature will be directly related to the complexity of the device, the simplest signature being derived from a single PN junction. For a complex integrated circuit on the other hand the signature will be complex depending upon lead selection, and biasing. Since any multi-leaded device may be interrogated through any two leads or any two sets of leads, the number of combinations of lead or lead set-pairs will increase rapidly with the total number of leads on the device, and, of course, the total number of leads on a device increases with device complexity. An important function of an associated computer would be the application of an elaborate interrogation program to a complex multi-leaded integrated circuit. The detailed development of such an interrogation program will be determined by the design and structural details of the given device under study.

7.3 Optical Excitation Program for Device

In a complicated integrated circuit or LSI structure, not all device elements within the circuit will be directly accessible to the external pin-out leads. In general, some of the device elements will be isolated by "outer layers" of circuitry and therefore may not be directly accessible. Flaws in such devices of course will not appear in the signature display. Auxiliary light probes to excite individually selected circuit elements during the chip excitation period can produce a continuous circuit to an "inner" isolated

device of interest. An appropriate timing program applied to the auxiliary light probes will thus allow a more complete and meaningful device electrical signature to be developed. The generation and application of that auxiliary light probe program constitutes an additional computer function.

7.4 Inventory of Characteristic Fault Signatures

Another important computer function is the cataloging of a large number of empirically derived signatures corresponding to known device flaws. The computer would compare a given device signature with the catalog of signatures contained within its memory bank in order to arrive at a go-no-go decision. For rejection or acceptance of the part. An important technical study function which must be accomplished in relation to any given device is the generation of characteristic signatures produced by known flaws, their evaluation as to device functional significance and the determination of acceptance criteria for use by the computer in device acceptance or rejection. This necessary research program for any given device would, in effect, constitute a reliability-oriented technical review of that device.

7.5 Blanking Functions

The amount of information generated in fully exciting a chip surface can be rather large. Not all of that information will necessarily be significant in assessing the quality of the unknown chip under examination. For example, certain non-recurring systematic errors in device fabrication may generate a large signal in the signature display. That signal may not be significant however, as in the case, for example, of a mask mis-alignment in a collector or emitter diffusion step. The impossibility of achieving perfect registration of the unknown and the reference chip images under these circumstances will result in a "signature" which is without significance from the standpoint of device quality. Other sources of such spurious and meaningless signals due to sequential mask mis-registration within process specification limits however, could conceivably result in device signatures of no significance. It is therefore suggested that a blanking or electronic masking function be provided, originating in and controlled by the associated computer support capability. This approach of eliminating "uninteresting" information is in

conformity with the basic reference chip concept itself by means of which the basic design criteria information in the chip which is of no interest, is eliminated from the final signature by subtracting the reference chip component.

7.6 Device Alignment Functions

The problem of reference image registration in a comparison system is a very critical one and reduces to two fundamental computer controlled functions:

1. Gross Chip Image Registration (Coarse Alignment). This function is basically one of pattern recognition and performed manually in initial system feasibility demonstration. Later improvements could result in computer implementation of this function.

2. Fine Adjustment Control. This function is essentially one of finding and continuously maintaining a minimum response in the reference and unknown chip difference signal. The implementation of this function assumes the existence of an electro-mechanical fine trim effector mechanism in order to achieve and continuously maintain as near perfect alignment of reference and unknown chip image as possible. This function is necessary in order to defeat the effects of mechanical vibration, thermal expansion and contraction, etc. in the mechanical alignment system.

   The mechanical servo-elements for use in the registration trimming function, could consist of piezo-electric deflector elements capable of small mechanical amplitude displacements arranged in such a manner as to allow small (trimming x-y and polar) movement on one of the mechanical stages shown in Figure 8.

7.7 Computer Memory Replacement of Reference Chip

The block of information represented by the reference chip could conceivably be stored within the memory bank of a computer, thus dispensing with the need for a physical reference chip and it's associated problems. Among the difficulties that would be resolved here would be the following:

1. There would be no need to find a "perfect" reference chip. Only the idealized device design data free of any processing flaw information which would be present in any real reference chip would be used in generating the unknown chip signature. This improved signature would thus represent more accurately the defect or flaw condition of the chip under examination and would be free of reference chip error effects.

2. The need for expensive, unreliable and cumbersome electro-mechanical alignment fixturing would be eliminated since the reference unknown chip opto-mechanical alignment would be replaced by a purely electrical function within the computer system.

3. The examiniation of a wide number of chips of varying designs would be facilitated by eliminating the need for mechanical replacement of reference chips.

Although it would appear reasonable that the reference chip could ultimately be replaced by a computer program, it is believed for the purpose of an experimental feasibility demonstration, that the physical reference chip approach be retained at this time for the following reasons:

1. In developing the physical significance of the signature it is believed that the presence of a real reference chip would be beneficial.

2. There is a backlog of existing opto-mechanical alignment technique and hardware developed for other chip comparison systems which would be available for application in this proposed approach.

3. The expense of developing a software package replacement for the reference chip will be large.

7.8 Computer Controlled System Approach

A simplified block diagram of a possible fully computerized system to automate the electromagnetic screening approach for high volume testing of semi-conductor devices is presented in Figure 11. This conceptual design of the computer test system is based on the following requirements:

- Capability for wide range of available lead-pair selections for device interrogation.
- Capability for pulsing the radiation source to an enhanced output level (i.e., 10X) during the test period according to any desired prearranged program.
- Condition the output signal (error signal) from the differential amplifier and compare this signal in relation to an inventory of stored "signatures" in memory (pattern recognition).
- Capability of controlling the blanking of the exciting raster.
- Control dwell time of raster (i.e., switch on and off).
- Program auxiliary continuous (non rastered) light sources for individual circuit element excitation in I.C. examination.

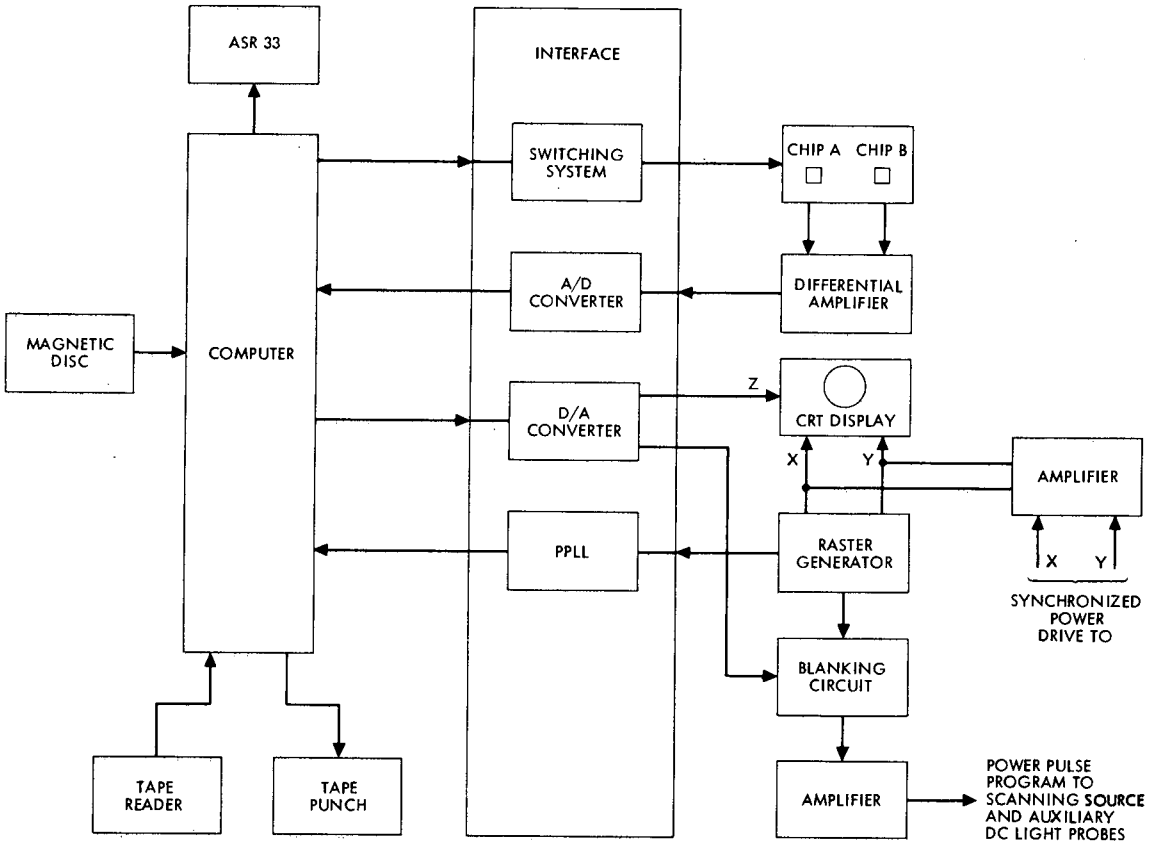

Figure 11. Block diagram of computer integrated scanning comparison system.

8.0 CONCLUSIONS AND RECOMMENDATIONS

This study has undertaken an evaluation of a number of technical approaches to semiconductor device inspection and evaluation employing electromagnetic radiation over the spectral range from x-ray to radio frequency. A review of the effects of various radiation wavelengths indicates that the optical spectrum including ultraviolet, visible and infrared radiation has the highest potential for success for the following reasons:

1. Quantum equivalent energy covers a range somewhat above and below that of the bandgap energy for semiconductors of interest and is therefore capable of exciting electrical carriers fully across the forbidden gap or into or out of midgap traps.
2. Resolution limits posed by wavelength considerations are such as to allow resolution of semiconductor device structural flaws.
3. The ready availability of convenient optical processing techniques and well defined radiation sources. In this range coherent and non-coherent monochromatic light generators are readily available.
4. By selecting light sources in the red and infra-red portions of the spectrum, it is possible to obtain various degrees of penetration of exciting radiation into silicon and other typically used semiconductors. Thus, this makes it possible to observe surface and near surface faults in semiconductors.
5. The ready availability of rastering techniques applicable to this spectral range allows easy scanning of device surfaces in order to resolve typical semiconductor flaws and simplify signal processing.

The x-ray portion of the spectrum offers the potential of penetrating the surface metallization to detect underlying flaws, however, x-rays also present the following limitations:

1. The high quantum equivalent energy of x-rays poses the problem of possible radiation damage to devices under examination.

2. The absorption coefficient for x-rays in semiconductors of interest in this study is low. The device silicon material would be effectively transparent to this radiation.

3. Severe experimental difficulties are involved in optically processing x-ray region radiation. Convenient means for focusing, collimating, beam shaping, small spot size limiting, spatial scanning, etc. are not available for this radiant energy range.

4. The large quantum energy of x-rays renders a simple interpretation of the events following photon absorption extremely difficult since many carriers are generated and complex secondary processes follow the primary photon absorption process.

5. Although the wavelength corresponding to x-radiation is of the order of size of the crystal lattice interval for semiconductors and could yield information as to the degree of "perfection" of the crystal, these wavelengths are extremely small compared with the dimensions of typical semiconductor processing flaws of interest in this study. Consequently, such flaws would not be expected to scatter, diffract or otherwise interact with x-ray radiation significantly.

The RF portion of the spectrum is significantly limited in applicability to semiconductor screening. The two major limitations are:

1. The quantum equivalent energy of this portion of the electromagnetic spectrum is a minute fraction of a typical semiconductor bandgap energy and in fact is much less than the quantum equivalent of the ambient thermal energy. Hence, RF would not be effective in generating electrical carriers or in significantly modifying their behavior.

2. The wavelength of even the highest frequency RF is much too long to resolve flaws of significance.

This study suggests that electromagnetic screening of semiconductors can be achieved with an optical (laser) scanning system employing a reference chip approach. In such a system, the photo response of a reference chip would be subtracted from that of an unknown chip to yield a display of those details in which the two chips differ in structure. Although it is premature to consider in detail at this time, it should be pointed out that existing computer aided pattern recognition, device design, device testing and information storage and retrieval techniques would be applicable to such an instrument. The ultimate objective could be the development of a completely automatic inspection tool for semiconductor device final as well as in-process evaluation, inspection and failure analysis functions.

It is not a proper conclusion of this study to indicate that the scanning approach recommended herein represents a panacea solution to automatic testing and inspection of semiconductor device chips. The signatures obtained for a given device are large in number depending upon the many ways in which a device may be stimulated and interrogated. In addition, any given signature will be complex in relation to the complexity of the device configuration on the one hand, and the intricacy of its processing history on the other. The resultant complexity of the signature may not yield to simple physical analysis. It will however, possess an empirical character which will serve to individually identify that device in terms of its flaw and defect configuration.

It is certainly possible to improve the relevancy of a given signature by using various cancellation techniques to remove from the signature common uninteresting information not related to device defects. The reference chip concept itself does this specifically with regard to device design geometry information, but other "information upgrading" techniques are also available and should be explored further.

On the basis of the understanding derived from this study, the scanning laser approach to device inspection appears to be sound, but not necessarily simple in implementation. This is particularly true relative to more complex device structures. The conclusion is certainly warranted, however, that the electromagnetic stimulation technique is potentially a very powerful one. Therefore, it is recommended that a first order experimental feasibility program be undertaken to develop characteristic device signatures employing the reference chip and radiation flooding approach. The devices selected for study in this first instance should be discrete and simple integrated structures containing known flaws in order to simplify the task of physical interpretation of developed signatures.

9.0 BIBLIOGRAPHY

1. John, M. F.: Silicon Power Device Material Problems. Proc. IEEE, vol. 55, no. 8, August 1967, pp. 1249-1271.

2. Black, J. F., et al: Scanned-Laser Microscope for Photoluminescense Studies. Appl. Optics, vol. 11, no. 7, July 1972, pp. 1553-1562.

3. Blech, I. A., et al: X-Ray Surface Topography of Diffusion-Generated Dislocations. Appl. Phys. Ltrs., vol. 7, no. 6, September 15, 1965, pp. 176-178.

4. Chaudhuri, A. R., et al: Velocities and Densities of Dislocations in Germanium and Other Semiconductor Crystals. Jour. Appl. Phys., vol. 33, no. 9, September 1962, pp. 2736-2746.

5. Everhart, T. E., et al: Evaluation of Passivated Integrated Circuits Using the Scanning Electron Microscope. Jour. Electrochem. Soc. vol. 111, no. 8, August 1964, pp. 929-936.

6. Fairfield, J. M., et al: Stress Effects in Masking Films on Silicon. Electrochemical Technology, vol. 6, no. 3-4; March-April 1968, pp. 110-113.

7. Fairfield, J. M. and Schwuttke, G. H.: Strain Effects Around Planar Diffused Structures. Jour. Electrochem. Soc., Solid State, vol. 115, no. 4, April 1968, pp. 415-422.

8. Gaylord, J. W.: Microplasma Observations in Silicon Junctions Using a Scanning Electron Beam. Jour. Electrochem. Soc., vol. 113, no. 7, July 1966, pp. 753-754.

9. Gupta, D. C., et al: Semiconductor Testing Using Scanned Laser Techniques. Solid State Technology, vol. 14, March 1971, pp. 44-50.

10. Haberer, J. R.: Photoresponse Mapping of Semiconductors. Phys. of Failure in Electronics, vol. 5, 1966. AD 655397.

11. Haberer, J. R. and Bart, J. J.: Charge Induced Instability in 709 Operational Amplifiers. Phys. of Failure Symposium, Las Vegas, Nev., 1972, pp. 106-111.

12. Haitz, R.H., et al: Avalanche Effects in Silicon p-n Junctions. Jour. Appl. Phys., vol. 34, no. 6, June 1963, pp. 1581-1590.

13. John, H.F., et al: Microinhomogeneity Problems in Silicon. IEEE Trans. Parts, Materials and Packaging, vol. PMP-2, no. 3, September 1966, pp. 51-58.

14. Kanai, Y.: The Change in Electron Mobility in Indium Antimonide at Low Electric Field. Jour. Phys. Soc. Jap. vol. 15, no. 5, May 1960, pp. 830-835.

15. Lander, J.J., et al: Microscopy of Internal Crystal Imperfections in Si p-n Junction Diodes by Use of Electron Beams. Appl. Phys. Ltrs., vol. 3, no. 11, December 1, 1963, pp. 206-207.

16. Lang, A.R.: Direct Observation of Individual Dislocations by X-Ray Diffraction. Jour. Appl. Phys., vol. 29, 1958, pp. 597-598.

17. Lang, A.R.: Studies of Individual Dislocations in Crystals by X-Ray Diffraction Microradiography. Jour. Appl. Phys., vol. 30, no. 11, September 1959, pp. 1748-1755.

18. Lawrence, J.E.: Behavior of Dislocations in Silicon Semiconductor Devices: Diffusion, Electrical. Jour. Electrochem. Soc., Solid State, vol. 115, no. 8, August 1968, pp. 860-865.

19. Libby, H.: Pulse Methods. Chapter 8 in "Introduction to Electromagnetic Nondestructive Test Methods." Wiley-Interscience, New York, N.Y., 1971.

20. McMahon, R.E.: A Laser Scanner for Integrated Circuit Testing. Phys. of Failure Symposium, Las Vegas, Nev., 1972, pp. 23-25.

21. Potter, C.N. and Sawyer, D.E.: Optical Scanning Techniques for Semiconductor Device Screening and Identification of Surface and Junction Phenomena. Phys. of Failure in Electronics, vol. 5, 1966. AD 655397.

22. Potter, C.N. and Sawyer, D.E.: A Flying-Spot Scanner. Rev. Sci. Inst., vol. 39, no. 2, February 1968, pp. 180-183.

23. Prussin, S.: Generation and Distribution of Dislocations by Solute Diffusion. Jour. Appl. Phys., vol. 32, no. 10, October 1961, pp. 1876-1881.

24. Queisser, H.J., et al: Diffusion Along Small-Angle Grain Boundaries in Silicon. Phy. Rev., vol. 123, no. 4, August 15, 1961, pp. 1245-1254.

25. Queisser, H.J.: Slip Patterns on Boron-Doped Silicon Surfaces. Jour. Appl. Phys., vol. 32, no. 9, September 1961, pp. 1776-1780.

26. Quiesser, H.J., and Finch, R.H.: Stacking Faults in Epitaxial Silicon. Jour. Appl. Phys., vol. 33, no. 4, April 1962, pp. 1536-1537.

27. Queisser, H.J.: Properties of Twin Boundaries in Silicon. Jour. Electrochem. Soc., vol. 110, no. 1, January 1963, pp. 52-56.

28. Roberts, F. and Young, J.Z.: The Flying-Spot Microscope. Proc. Inst. Elect. Eng. London, vol. 99, Part III A, 1952, pp. 747-757.

29. Robinson, P.H. and Dumin, D.J.: The Deposition of Silicon on Single-Crystal Spinel Substrates. Jour. Electrochem. Soc., Solid State, vol. 115, no. 1, January 1968, pp. 75-78.

30. Rupprecht, H. and Schwuttke, G.H.: Distribution of Boron-Induced Defects in Shallow Diffused Surface Layers of Silicon. Jour. Appl. Phys., vol. 37, no. 7, June 1966, pp. 2862-2866.

31. Sato, Y. and Arata, H.: Distribution of Dislocations near the Junction Formed by Diffusion of Phosphorus in Silicon. Jap. Jour. Appl. Phys., vol. 3, no. 9, September 1964, pp. 511-515.

32. Schwuttke, G.H. and Queisser, H.J.: X-Ray Observations of Diffusion-Induced Dislocations in Silicon. Jour. Appl. Phys., vol. 33, no. 4, April 1962, pp. 1540-1542.

33. Schwuttke, G.H.: New X-Ray Diffraction Microscopy Technique for the Study of Imperfections in Semiconductor Crystals. Jour. Appl. Phys., vol. 36, no. 9, September 1965, pp. 2712-2721.

34. Schwuttke, G.H. and Fairfield, J.M.: Dislocations in Silicon Due to Localized Diffusion. Jour. Appl. Appl. Phys., vol. 37, no. 12, November 1966, pp. 4394-4396.

35. Schwuttke, G.H. and Howard, J.K.: X-Ray Stress Topography of Thin Films on Germanium and Silicon. Jour. Appl. Phys. vol. 39, no. 3, February 1968, pp. 1581-1591.

36. Sherman, B. and Black, J.F.: Scanned Laser Infrared Microscope. Appl. Optics, vol. 9, no. 4, April 1970, pp. 802-809.

37. Spitzer, W.G. and Fan. H.Y.: Infrared Absorption in n-Type Silicon. Phy. Review, vol. 108, no. 2, October 15, 1957, pp. 268-271.

38. Spitzer, W.G. and Whelan, J.M.: Infrared Absorption and Electron Effective Mass in n-Type Gallium Arsenide. Phy. Review, vol. 114, no. 1, April 1, 1959, pp. 59-63.

39. Stanford, E.G., et al: Progress in Applied Materials Research. Vol. 6, Gordon and Breach, Science Publishers, 1964.

40. Tihanyi, J. and Pasztor, G.: Observation of Surface Phenomena on Semiconductor Devices by a Light Spot Scanning Method. Solid State Elect., vol. 10, 1967, pp. 235-239.

41. Washburn, J., et al: Diffusion-Induced Dislocations in Silicon. Jour. Appl. Phys., vol. 35, no. 6, June 1964, pp. 1909-1914.

42. Weissman, S.: Method for the Study of Lattice Inhomogeneities Combining X-Ray Microscopy and Diffraction Analysis. Jour. Appl. Phys., vol. 27, no. 4, April 1956, pp. 389-395.

43. International Business Machines Corp., Crystal Properties as Influenced by Crystallographic Imperfections. AFCRL-70-0110, March 2, 1970.

44. Research Triangle Institute, Fabrication of the Video Prototype Machine. AFWL-TR-71-106, January 1972.

45. Research Triangle Institute, Operation and Maintenance Manual Microelectronic Wafer and Integrated Circuit Test Set, TTU-311/E (XV-1). AFWL-TR-71-122, January 1972.

46. Tropel, Inc. Interim Technical Report. Jet Propulsion Laboratory Subcontract No. 953152, November 10, 1971.